REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 1 to recite that only a portion of the semiconductor substrate, at the upper end portion of the trench, and not other portions of the semiconductor substrate lining the trench, is oxidized, so as to provide a curvature of the upper end portion of the trench. Claims 2, 4, 5 and 10 have been similarly amended. In addition, claim 9 has been amended to recite that in forming an insulating film inside the oxidized trench regions, completely filled trench regions are thereby formed; and to recite that the second oxidation is performed to selectively oxidize only an opening side of the completely filled trench regions in the substrate. Claim 15 has been amended, in step (e), to recite that in removing the buried insulation film formed on the oxidation prevention film, the buried insulating film is left in the trench. In connection with these amendments to previously considered claims, note, for example, the paragraph bridging pages 14 and 15 of Applicants' specification.

Furthermore, claims 3 and 6 have been amended to recite a step for forming trenches having a predetermined depth, consistent with respective parent claims 2 and 5.

In addition, Applicants are adding new claims 39-48 to the application.

Claims 39 and 40, each dependent on claim 15, respectively recites that after the step of removing the buried insulating film (formed on the oxidation prevention film) and prior to the step of removing the oxidation prevention film, the method includes the further step of performing oxidation of the substrate only at the upper end portion of this trench, and the method includes the further step of selectively oxidizing the semiconductor substrate at the upper end portion of the trench, to increase the curvature of the upper end portion of the trench as compared with the curvature provided in step (c).

Claim 41 corresponds to previously considered claim 1, but additionally recites that in the oxidizing step (c), a curvature of the upper end portion of the trench is formed; and to recite in step (e) that after burying the buried insulating film, the semiconductor substrate is selectively oxidized at the upper end portion so as to provide an increased curvature of the upper end portion of the trench as compared with the curvature formed in step (c). Claim 42, dependent on claim 41, recites that the step (f) of removing the buried insulating film is performed before the step (e) of selectively oxidizing the substrate, and the step (g) of eliminating the oxidation prevention film is performed after the step (e) of selectively oxidizing the semiconductor substrate at the upper end portion.

Claim 43 corresponds to previously considered claim 2, but recites, in step (f), selectively oxidizing the semiconductor substrate after burying the buried

insulating film, so as to increase the radius of curvature at the corners of the shallow trenches as compared with the radius of curvature formed in step (b). Claim 44, dependent on claim 43, recites that the step (g) of removing the buried insulating film is performed prior to the step (f) of selectively oxidizing, and the step (h) of eliminating the oxidation prevention film is performed after the step (f) of selectively oxidizing.

Independent claims 45-47 respectively correspond to claims 4, 9 and 10 of the previously considered claims. Claim 45, as compared with previously considered claim 4, recites that in the oxidizing step (c), a curvature is provided at the upper portions of the trenches; and to recite in step (f) selectively oxidizing the semiconductor substrate. Claim 46, as compared with previously considered claim 9, additionally recites that the performing of the first oxidation in step (c) provides a curvature at an opening side of the trench regions; and to recite, in step (e), performing a selective second oxidation to selectively oxidize the opening side of the completely filled trench regions in the substrate, so as to provide an increased curvature at the opening side as compared to said curvature provided in step (c). Claim 47, as compared with previously considered claim 10, additionally recites that the oxidizing step (c) provides the upper end portion of the trench with a radius of curvature; and that, in step (e), the upper end portion of the trench is provided with an increased radius of curvature, as

compared with the radius of curvature provided in step (c), by selectively oxidizing the upper end portion of the trench. Claim 48, dependent on claim 47, recites that the step (f) of removing the buried insulating film is performed prior to the step (e) of providing the upper end portion of the trench with an increased radius of curvature; and the step (g) of removing the oxidation prevention film as performed after the step (e) of providing the upper end portion of the trench with an increased radius of curvature. See, for example, the sole full paragraph on page 14, and the paragraph bridging pages 14 and 15, together with page 23, line 3 to page 25, line 4, of Applicants' specification.

The objection to claim 16 under 37 CFR §1.75(c), and set forth in Item 2 on page 2 of the Office Action mailed August 28, 2001, is noted. Applicants traverse this objection to claim 16, and respectfully contend that the recitation in previously considered claim 16 further defined the subject matter of claim 15, in defining the <u>shape</u> of the oxidized part at the upper portion of the trench. In connection with claim 16, note also claim 12. In any event, in order to facilitate proceedings in connection with the above-identified application, Applicants are presently canceling claim 16 without prejudice or disclaimer of the subject matter thereof.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patently distinguish over the teachings of the

documents applied by the Examiner in rejecting the claims formerly in the application, that is, the teachings of the U.S. Patents to Mehta, No. 5,679,599, and to Park et al., No. 5,885,883, Japanese Patent Document No. 01-107554, and the publication by Lee et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation" in the <u>1996 Symposium on VRSI Technology Digest of Technical Papers</u> (1996), pages 158 and 159, under the provisions of 35 USC §103.

Initially, it is noted that the date, for prior art purposes, of U.S. Patent No. 5,885,883 to Park et al., is April 15, 1997, <u>after</u> the filing date of the Japanese priority application for the above-identified application (that is, after September 17, 1996). Moreover, note that the date alleged by the Examiner, for prior art purposes, of the article by Lee et al., is 1996; it is respectfully submitted that under present procedures, without a month or date, such 1996 date is December 31, 1996, <u>after</u> the filing date of the Japanese priority application for the above-identified application. As acknowledged by the Examiner in the Office Action mailed August 28, 2001, in the above-identified application, a claim for foreign priority under 35 USC §119 has been made in the above-identified application, and the necessary copy of the priority document has been received. In addition, enclosed herewith is an English translation of the Japanese priority application for the above-identified application, together with a Declaration as to accuracy

of the translation. As is clear from this enclosed English translation, all requirements of 35 USC §119, including the necessary description and enablement under 35 USC §112, are satisfied by this Japanese priority application, for the subject matter claimed in the above-identified application. Accordingly, the above-identified application should be accorded benefit of the filing date of the Japanese priority application for the above-identified application. Moreover, by the filing of the enclosed English translation with Declaration as to accuracy of the translation, all procedural requirements of 37 CFR §1.55 have been satisfied.

In view of the foregoing, it is respectfully submitted Lee et al. and Park et al. do <u>not</u> constitute prior art in connection with the presently claimed subject matter. For this reason alone, reconsideration and withdrawal of the rejections set forth in Items 3, 4 and 7-10 of the Office Action mailed August 28, 2001, is respectfully requested.

In any event, it is respectfully submitted that the teachings of the applied documents would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including, after burying the buried insulating film, oxidizing only a portion of the semiconductor substrate, at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate than the upper end

portion of the trench, so as to provide a curvature, or increased curvature, at the upper end portion of the trench. See claim 1; note also claims 2, 4, 5, 10 and 39. Note also claim 9, reciting a second oxidation to selectively oxidize only an opening side of the completely filled trench regions in the substrate.

Furthermore, it is respectfully submitted that the applied documents would have neither taught nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including the selective oxidation of the semiconductor substrate at the upper end portion or at upper corners of the trench, after burying the buried insulating film. See claims 41, 43 and 45-47; see also claims 9 and 40.

Moreover, it is respectfully submitted that these applied documents would have neither taught nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including wherein the buried insulating film formed on the oxidation film is removed prior to oxidizing the substrate after burying the buried insulating film, with the oxidation prevention film being eliminated after the selective oxidation of the substrate. See claims 14, 42, 44 and 48; note also, for example, claims 4 and 5, reciting that only a portion of the substrate at the upper end portions of the trenches is oxidized, after the buried insulating film formed on the oxidation prevention film is removed.

Furthermore, it is respectfully submitted that the teachings of the applied documents would have neither taught nor would have suggested such a method as in the present claims, including oxidizing a trench portion formed in a substrate so as to provide the upper end portion of the trench with a curvature, burying a buried insulating film into the trench, removing the buried insulating film formed on the oxidation prevention film and removing the oxidation prevention film on the circuit formation surface of the substrate. See claim 15.

In addition, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining, dependent claims, having the processing as discussed previously, and additionally wherein shallow trenches are formed by isotropic etching and the trenches having the predetermined depth are formed by anisotropic etching (see claims 3 and 6); and/or wherein the buried insulating film is made of material, or is made by a processing technique, as set forth in claims 18-38; and/or wherein an angle between the circuit formation surface of the substrate and a side surface of the semiconductor substrate forming the trench is within a range as in claim 13; and/or wherein the oxidizing the trench portion to provide the upper end portion of the trench with a curvature is a thermal oxidation (see claim 17).

The invention as presently claimed in the above-identified application is

directed to a method of manufacturing a semiconductor substrate, or semiconductor device, having a trench isolation structure. A so-called "trench isolation structure" made by a selective oxidation method, which forms trenches extending into the substrate from the substrate surface and then selectively oxidizes the trenches to form a thermal oxide film, has been employed as the insulation/isolation structure of semiconductor devices, as described in the paragraph bridging pages 1 and 2 of Applicants' specification.

In the trench isolation structure, end points (corner points) essentially exist near the trench upper end portion of the semiconductor substrate. Stress concentration fields (both mechanical stress and electrical stress) are formed near the end points. Because such stress concentration fields are formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape having an acute angle, as shown by the structure represented by reference character 4 in Fig. 1C of Applicants' disclosure. If such an acute angle portion 4 remains on the semiconductor surface, however, concentration of electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of transistors, capacitors, etc., formed utilizing such substrate. Moreover, mechanical stress fields, which are disadvantageous, are also formed. See the paragraph bridging pages 3 and 4 of Applicants' specification.

Against this background, Applicants provide a process wherein trench isolation can be utilized, without causing deterioration of breakdown voltage characteristics of transistors and capacitors utilizing the substrate with the trench isolation structure, while providing semiconductor devices having a high reliability. Moreover, Applicants fabricate such structure utilizing a relatively simple technique.

Applicants have found that the desired structure can be achieved by preventing a substrate shape in the proximity of the upper end portion of the device isolation trench from becoming an acute angle; and, by the present invention, provide simple techniques for preventing such acute angle. Specifically, according to the present invention, Applicants provide various procedures which can easily and effectively provide a curvature (increased curvature) only of an upper end portion of the trench, by selectively oxidizing only the upper end portion so as to prevent the aforementioned acute angle. For example, and specifically, according to the present invention, <u>after burying the buried insulating film</u>, the semiconductor substrate can be oxidized (selectively) at only the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench. Moreover, the semiconductor substrate can be oxidized <u>after the buried insulating film formed on the oxidation prevention film is removed</u>. Moreover, more generally, <u>after burying the buried</u>

<u>insulating film</u>, an upper end portion of the trench can be provided with the curvature (increased curvature). This prevention of the acute angle can be achieved, for example, by thermal oxidation of the upper end portion <u>only</u> of the trench; e.g., by forming bird's beaks at the upper end portion of the trench.

As is clear according to the specification of the present application, since the buried insulating film 9 (see, e.g., Fig. 2(g)) has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from near the trench upper end portion 12, and the inside of the trench is hardly oxidized. That is, a longer time is necessary for oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1, than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench side walls and the upper surface of the trench exists at the trench upper end portion 12, and oxidation seeds can diffuse at a relatively high rate along this weak boundary layer. As a result, oxidation seeds are supplied to the trench upper end portion 12 within a short time, so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is

promoted. Note, for example, the paragraph bridging pages 14 and 15 of Applicants' specification.

It is emphasized that according to the present invention, Applicants have recognized that curvature formation including, for example, at the upper end portion of the trench, is important to reduce concentration of both mechanical and electrical stress fields, in order to provide a reliable device with shallow trench insulation. Applicants provide simple techniques for increasing curvature (providing roundness) at the top corners of the trench, and, according to various aspects of the present invention, provide such increased curvature by, e.g., additional oxidation after filling the trench and prior to removal of the oxidation prevention film. Only a small amount of oxidation is utilized to provide the roundness at the upper corners of the trench (for example, the oxidation is performed for only a short time; and, according to various aspects of the present invention, the filler material (of, for example, chemical vapor deposited oxide) is removed prior to performing the additional oxidation to increase curvature), with the oxidation prevention film being removed <u>after</u> the additional oxidation.

Thus, according to the present invention, simple techniques are provided to achieve increased radius of curvature at top corners of the trench, so as to reduce concentration of both mechanical and electrical stress fields, so as to provide reliable semiconductor devices.

As established previously, neither of the U.S. Patent to Park et al. or the publication by Lee et al., constitutes prior art in connection with the presently claimed subject matter. In any event, the teachings of these two applied references would have neither taught nor would have suggested increased curvature formation to reduce concentration of both mechanical and electrical stress fields, and the processing techniques for increasing the curvature, for providing sufficient curvature, according to the present invention.

In particular, the article by Lee, et al. reports on a comparison of densification methods using H_2O and N_2 ambient annealing of filled CVD oxide for quarter micron shallow trench isolation (STI). This article discloses that a densification in the oxidizing ambient causes an unwanted side wall oxidation, which in turn exerts an extreme stress toward the active Si area of the devices, and that if this stress surpasses the yield stress of the silicon they form crystallographic defects such as dislocations which increase the leaking current of the STI. The article discloses experimentation wherein at first field and active regions are defined by photolithography and etch steps. Trench side wall oxide was grown, and CVD oxide was deposited to fill the trenches, and two densification processes were performed separately (one in H_2O ambient and the other in N_2 ambient). Chemical Mechanical Polishing was then applied to planarize the CVD oxide until SiN was exposed, the SiN layer was subsequent

removed in phosphoric acid, and channel stop implantation was carried out. Then, the pad oxide was removed in a diluted HF solution. In the results shown in this article, N^+/P junction leakage currents occurred in H_2O densification, the leakage currents increasing as the isolation size becomes smaller. On the other hand, no increase in the leakage current occurred upon densification in the N_2 ambient.

This article is concerned with densification, and discloses advantages achieved utilizing an inert (N_2) ambient. In any event, relatively long annealing is performed for densification; and it is respectfully submitted that this article would have neither taught nor would have suggested the selective oxidation, or oxidation substantially only at the upper end portions of the trench, and advantages achieved thereby, as described in the foregoing.

Park et al. discloses methods of forming electrically isolated semiconductor active regions in the semiconductor substrate. The methods include forming trenches at a face of a semiconductor substrate and then filling the trenches with electrically insulating regions. In order to prevent exposure of those portions of the substrate extending adjacent the trenches, supplemental oxide regions are formed at the interfaces between the upper portions of the trench side walls and the electrically insulating regions in the trenches, by exposing the electrically insulating regions to an oxidation atmosphere at a

temperature in the range between about 950°C and 1100°C. Note column 2, lines 35-46. Note also column 2, lines 46-50. Note further column 3, lines 28, 29, 32 and 45-65; and column 4, lines 20-22.

It is respectfully submitted that Park et al. focuses on providing structure to avoid exposure of the semiconductor substrate at the trench side walls, and does not, e.g., focus on rounding of the upper corners to reduce mechanical and electrical stress fields and improve reliability of the formed device with shallow trench insulation.

As for the proper prior art as applied by the Examiner, Mehta discloses a combination of trench isolation and local oxidation of the silicon isolation processes. See column 1, lines 8-10. The process comprises forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the semiconductor substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate, and thermally growing a field oxide in the first and second isolation regions. Note the paragraph bridging columns 3 and 4 of this patent. See also column 4, lines 47-51; column 5, lines 37-42 and 64-67; and column 6, lines 4-9 and 19-23.

In connection with application of Mehta to claims 4 and 24-26, it is emphasized that claim 4 as presently amended recites oxidizing only a portion of the semiconductor substrate at the upper end portions of the trenches, and not substantially portions of the semiconductor substrate lining the trenches. On the other hand, note that in the field oxide oxidation in Mehta, a relatively thick oxide is provided, requiring relatively long oxidation time, which would act to oxidize substantially the entire substrate surface lining the trench. It is respectfully submitted that Mehta would have neither taught nor would have suggested the presently claimed invention, including oxidation of only a portion of the semiconductor substrate at the upper end portions of the trenches, or the selective oxidation, as in the present claims.

In connection with claims 5, 6 and 27-29, it is respectfully submitted that the additional teachings of Japanese Patent Document No. 1-107554 would not have rectified the deficiencies of Mehta, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art. Japanese Patent Document No. 1-107554 discloses a technique to obtain a semiconductor device in which an oxide film is easily buried, by forming a taper opening of the trench. This patent document, as seen by the abstract thereof, discloses that with an oxide film 2 as a mask, a silicon substrate 1 is isotropically plasma-etched, and a recess of circular-arc-shaped section is formed; further, the

recess is anisotropically etched with the film 2 of a mask, to form a trench 3 of a desired depth, with the film 2 of the mask then being removed; and then, the formed trench has a taper 3a in the opening.

Even assuming, *arguendo*, that the teachings of the Japanese Patent Document and Mehta were properly combinable, such combined teachings would have neither disclosed nor would have suggested the subject matter as in the present claims, including, *inter alia*, the oxidation of only a portion of the semiconductor substrate extending from the corners, or the selective oxidation of the semiconductor substrate, and the advantages achieved thereby in providing the increased radius of curvature, or other aspects of the present invention as discussed in the foregoing, including wherein the selective oxidation, or oxidizing only a portion of the semiconductor substrate, is performed after removing the buried insulating film formed on the oxidation prevention film.

In view of the foregoing comments and amendments, and further in view of the enclosed English translation with Declaration of accuracy, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made in the claims by the current Amendment. This marked-up version is on the attached pages, the first page of which is captioned "Version with Markings to Show Changes

Made".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 500.36904X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Thrice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, said trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench;

(d) burying a buried insulating film into said trench so oxidized;

(e) after burying said buried insulating film, oxidizing only a portion of said semiconductor substrate, at said upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, so as to provide a curvature of the upper end portion of the trench;

(f) removing said buried insulating film formed on said oxidation prevention film;

(g) eliminating said oxidation prevention film formed on said

semiconductor substrate; and

(h) after said eliminating, forming a gate oxide film.

2. (Thrice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth to said shallow trenches having a radius of curvature so formed;

(d) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(e) burying a buried insulating film into said trenches so oxidized;

(f) oxidizing <u>only a portion of</u> the semiconductor substrate <u>extending from said corners, and not substantially at other portions of the semiconductor substrate lining the trenches</u>, after burying said buried insulating film, so as to increase the radius of curvature of the shallow trenches;

(g) removing said buried insulating film formed on said oxidation

prevention film;

(h) eliminating said oxidation prevention film formed on said semiconductor substrate; and

(i) after said eliminating, forming a gate oxide film.

3. (Amended) A method of fabricating a semiconductor device according to claim 2, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming [a] trenches having a predetermined depth is carried out by anisotropic etching.

4. (Thrice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming trenches having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate, said trenches having upper end portions not covered by said oxidation prevention film;

(c) oxidizing trench portions formed in said semiconductor substrate, exposed in said trenches;

(d) burying a buried insulating film into said trenches so oxidized;

(f) oxidizing <u>only a portion of</u> said semiconductor substrate <u>at said upper end portions of said trenches, and not substantially at other portions of the semiconductor substrate lining the trenches,</u> after said buried insulating film formed on said oxidation prevention film is removed, said upper end portions not covered by said oxidation prevention film being oxidized;

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate; and

(h) after said oxidizing said semiconductor substrate, forming a gate oxide film.

5. (Thrice Amended) A method of fabricating as semiconductor substrate comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in desired positions of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth in said shallow trenches having a radius of curvature;

(d) oxidizing trench portions formed in said semiconductor substrate,

exposed in said trenches;

(e) burying a buried insulation film into said trenches so oxidized;

(f) removing said buried insulating film formed on said oxidation prevention film;

(g) oxidizing <u>only a portion of</u> said semiconductor substrate <u>extending from said corners, and not substantially at other portions of the semiconductor substrate lining the trenches,</u> after said buried insulating film formed on said oxidation prevention film is removed, so as to increase the radius of curvature of the shallow trenches at said corners;

(h) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate; and

(i) after said oxidizing said semiconductor substrate, forming a gate oxide film.

6. (Amended) A method of fabricating a semiconductor device according to claim 5, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming [a] trenches having a predetermined depth is carried out by anisotropic etching.

9. (Thrice Amended) A method of fabricating a semiconductor device

comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate,

(b) forming trench regions in said substrate from said circuit formation surface thereof,

(c) performing a first oxidation to form an oxide film on said trench regions formed in step (b), and

(d) forming an insulating film inside said oxidized trench regions so as to completely fill them, thereby forming completely filled trench regions,

characterized by further steps of:

(e) performing a second oxidation to selectively oxidize only an opening side of said completely filled trench regions in said substrate; and

(f) after performing the second oxidation, forming a gate oxide film.

10. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

~~(a) forming an oxidation prevention film on a circuit formation surface~~ of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, the trench

having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench;

(d) burying a buried insulating film into said trench so oxidized;

(e) after burying said buried insulating film, [providing] oxidizing only a portion of the semiconductor substrate, at the upper end portion of said trench and not substantially at other portions of the semiconductor substrate lining the trench, to provide the upper end portion with a curvature;

(f) removing said buried insulating film formed on said oxidation prevention film; and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

15. (Twice Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate, the trench

having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in said semiconductor substrate, exposed in said trench, so as to provide the upper end portion of said trench with a curvature;

(d) burying a buried insulating film into said trench so oxidized;

(e) removing said buried insulating film formed on said oxidation prevention film, having said buried insulating film in said trench; and

(f) removing said oxidation prevention film formed on the circuit formation surface of said circuit substrate.